CLAIMS:

1. A plasma oxidation process comprising:

exposing an oxidizable surface to an oxidizing plasma, wherein the oxidizing plasma has an activity relative to the oxidizable surface;

forming an oxide film on the oxidizable surface; and

regulating the oxidizing plasma activity to limit a rate of formation of the oxide film.

2. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises bombarding the oxidizable surface with energized ions prior to exposing the oxidizable surface to the oxidizing plasma.

3. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove contaminants from the oxidizable surface.

4. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove other oxide layers present on the oxidizable surface.

5. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to facet the oxidizable surface.

6. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface with energized ions comprises subjecting the oxidizable surface to a bias voltage.

7. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises diluting the oxidizing plasma with an inert gas.

8. The plasma oxidation process of claim 1 further comprising providing a substrate having a back surface opposite a face surface, wherein the oxidizable surface comprises at least a portion of the face surface, and wherein regulating the oxidizing plasma activity comprises contacting the back surface with a cooling medium.

9. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises applying an RF bias voltage to the oxidizable surface.

10. The plasma oxidation process of claim 1 further comprising:
providing a plasma chamber;
placing a substrate in the plasma chamber; and
igniting the oxidizing plasma after placing the substrate in the plasma chamber.

11. The plasma oxidation process of claim 1 further comprising igniting an inert gas plasma prior to igniting the oxidizing plasma.

12. The plasma oxidation process of claim 11 further comprising placing the oxidizable surface in the inert gas plasma.

13. The plasma oxidation process of claim 1 further comprising providing a plasma power source having an output power, and wherein regulating the oxidizing plasma comprises limiting the output power to a predetermined level.

14. The plasma oxidation process of claim 1, wherein the oxidizable surface comprises silicon.

15. The plasma oxidation process of claim 1, wherein the oxidizable surface comprises a semiconductor element of an antifuse device.

16. The plasma oxidation process of claim 1, wherein exposing an oxidizable surface to an oxidizing plasma comprises exposing the oxidizable surface to a plasma comprising oxygen.

17. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises applying a bias voltage and sputtering a portion of the oxide film while simultaneously forming the oxide film.

18. A process for fabricating an oxide film in a semiconductor device comprising the steps of:

forming a semiconductor layer;

exposing the semiconductor layer to a plasma comprising oxygen,

wherein the plasma has an activity relative to the semiconductor layer;

forming an oxide film on the semiconductor layer; and

regulating the plasma activity to limit a rate of formation of the oxide film.

19. The process of claim 18, wherein the step of forming a semiconductor layer comprises forming a doped semiconductor layer.

20. The process of claim 18, wherein the step of forming a semiconductor layer comprises forming a silicon layer.

21. The process of claim 18, wherein the step of forming a semiconductor layer comprises forming a germanium layer.

22. The process of claim 18 further comprising forming an electrically conductive layer prior to forming the semiconductor layer.

23. The process of claim 18, wherein the oxide film comprises a gate oxide layer.

24. The process of claim 18, wherein the oxide film comprises a passivation layer.

25. A process for fabricating a memory cell in a semiconductor device comprising the steps of:

forming a first electrically conductive layer;

forming a first semiconductor layer of a first conductivity type overlying the first electrically conductive layer;

forming an antifuse layer on the first semiconductor layer using a high density plasma oxidation process;

forming a second semiconductor layer of a second conductivity type overlying the antifuse layer; and

forming a second electrically conductive layer overlying the second semiconductor layer.

26. The process of claim 25, wherein the step of forming a first semiconductor layer comprises forming a silicon layer.

27. The process of claim 25, wherein the step of forming a first semiconductor layer comprises forming a layer of group III-V material.

28. The process of claim 27, wherein the step of forming a first semiconductor layer comprises forming a layer of gallium arsenide.

29. The process of claim 25, wherein the step of forming a first semiconductor layer comprises forming a germanium layer.

30. The process of claim 25, wherein the step of forming an electrically conductive layer comprises forming a metal layer.

31. The process of claim 25, wherein the step of forming an antifuse layer comprises:

exposing the first semiconductor layer to an oxidizing plasma, wherein the oxidizing plasma has an activity relative to the first semiconductor layer;

forming an oxide film on the first semiconductor layer; and

regulating the oxidizing plasma activity to limit a rate of formation of the oxide film.

32. The process of claim 31, wherein exposing an oxidizable surface to an oxidizing plasma comprises exposing the oxidizable surface to a plasma comprising oxygen.

33. A process for fabricating a dielectric rupture element in a semiconductor device comprising the steps of:

forming a first semiconductor layer of a first conductivity type;

subjecting the first semiconductor layer to a high density plasma comprising oxygen to form an oxide antifuse layer;

forming a second semiconductor layer having a second conductivity type in contact with the oxide antifuse layer; and

applying a voltage potential across the oxide antifuse layer sufficient to create an electrical current path between the first and second semiconductor layers.

34. The process of claim 30, wherein subjecting the first semiconductor layer to a high density plasma comprises:

subjecting the first semiconductor layer to an oxidizing plasma having an activity relative to the first semiconductor layer;

forming an oxide film on the first semiconductor layer; and

regulating the oxidizing plasma activity to limit a rate of formation of the oxide film.

35. A process for forming an antifuse comprising:

exposing an oxidizable surface to an plasma oxidation process for an initial exposure time; and

growing an oxide film on the oxidizable surface, and

wherein the plasma process is configured such that the oxide film grows to a predetermined thickness substantially independent of an exposure time beyond the initial exposure time.

36. The process of claim 35, wherein the plasma oxidation process comprises providing a substrate having a back surface opposite a face surface, wherein the oxidizable surface comprises at least a portion of the face surface, and contacting the back surface with a cooling medium.

37. The process of claim 35, wherein the plasma oxidation process comprises applying an RF bias voltage to the oxidizable surface.

38. The process of claim 35, wherein the plasma oxidation process comprises generating a plasma comprising oxygen and an inert gas.

39. The process of claim 35, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma oxidation process.

40. The process of claim 39, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

41. A process for fabricating a multi-level memory array comprising the steps of:

forming a conductive layer;

forming a semiconductor layer on the conductive layer,

wherein the semiconductor layer is doped with a first conductivity type dopant;

defining a plurality of spaced-apart rail-stacks and leaving a space therebetween;

filling the space between the plurality of spaced-apart rail-stacks with a dielectric material;

planarizing the semiconductor layer and the dielectric material to form a planarized surface; and

forming an antifuse layer having a predetermined thickness on the planarized surface using a high density plasma oxidation process.

42. The process of claim 41, wherein the step of forming an antifuse layer comprises growing the antifuse layer on the plurality of spaced-apart rail-stacks.

43. The process of claim 41, wherein the step of forming a semiconductor layer comprises forming a first semiconductor layer doped with a conductivity-determining dopant to a first concentration and forming a second semiconductor layer doped with the conductivity-determining dopant to a second concentration, and wherein the second concentration is less than the first concentration.

44. The process of claim 41, wherein the step of forming an antifuse layer comprises forming an oxide layer having a thickness of about 15Å to about 200Å.

45. The process of claim 41, wherein the step of forming an antifuse layer comprises exposing the planarized surface to an oxidizing plasma,

wherein the oxidizing plasma has an activity relative to the planarized surface and regulating the oxidizing plasma activity to limit a rate of formation of the antifuse layer.

46. A process for fabricating a multi-level memory array comprising the steps of:

forming a conductive layer;

forming a first silicon layer on the metal layer,

wherein the first silicon layer is doped with a first conductivity type dopant to a first concentration;

forming a second silicon layer on the first silicon layer,

wherein the second silicon layer is doped with the first conductivity type dopant to a second concentration, and

wherein the second concentration is less than the first concentration;

forming an antifuse layer on the second silicon layer using a high density plasma oxidation process;

forming a third silicon layer on the antifuse layer,

wherein the third silicon layer is doped with a second conductivity type dopant to a concentration greater than the second concentration;

defining first spaced-apart rail-stacks from the conductive layer, the first and second silicon layers, the antifuse layer and the third silicon layer and leave a space therebetween;

filling the space between the first spaced-apart rail-stacks with a dielectric material; and

planarizing an upper surface of the dielectric material and the third silicon layer.

47. The process of claim 46 further comprising repeating the steps of claim 44 to form second spaced-apart rail-stacks disposed above the first spaced-apart rail-stacks and oriented generally perpendicular to the first spaced-apart rail-stacks.

48. The process of claim 46 further comprising etching through the third silicon layer of the first spaced-apart rail-stacks using the second spaced-apart rail-stacks as an etching mask.

49. The process of claim 46 further comprising planarizing the second silicon layer prior to the step of forming an antifuse layer.

50. The process of claim 46, wherein the step of forming a conductive layer comprises forming a conductive layer having a thickness of about 500 Á to about 1500Á.

51. The process of claim 46, wherein the step of forming a first silicon layer comprises forming a silicon layer having a thickness of about 1000 Á to about 4000Á.

52. The process of claim 46, wherein the step of forming a second silicon layer comprises forming a silicon layer having a thickness of about 300Á to about 3000Á.

53. The process of claim 46, wherein the step of planarizing an upper surface of the dielectric material and the third silicon layer comprises reducing the thickness of the third silicon layer to about 300Á to about 2000Á.

54. The process of claim 46, wherein the step of forming an antifuse layer comprises forming a silicon dioxide layer to a thickness of no more than about 200Á.

55. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising an oxygen species and a nitrogen species,

wherein the plasma has an activity relative to the oxidizable surface;

forming an oxynitride film on the oxidizable surface; and

regulating the plasma activity to limit a rate of formation of the oxynitride film.

56. The process of claim 55, wherein the nitrogen species comprises a compound selected from the group consisting of nitrogen, ammonia and nitrous oxide.

57. The process of claim 55, wherein the step of forming an oxynitride film comprises a gate oxide layer.

58. The process of claim 55, wherein the step of forming an oxnitride film comprises a passivation layer.

59. The process of claim 55, wherein the step of forming an oxnitride film comprises an antifuse layer.

60. The process of claim 55, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising an oxygen species and a nitrogen species.

61. The process of claim 60, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

62. A process for fabricating an oxide film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising oxygen, wherein the plasma has an activity relative to the oxidizable surface;

forming an oxide film on the oxidizable surface;

regulating the plasma activity to limit a rate of formation of the oxide film; and

forming a silicon nitride layer overlying the oxide film.

63. The process of claim 62, wherein the step of forming a silicon nitride layer comprises plasma deposition of silicon nitride.

64. The process of claim 62, wherein the step of forming a silicon nitride layer comprises chemical vapor deposition of silicon nitride.

65. The process of claim 62, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.

66. The process of claim 65, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

67. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising an oxygen species,

wherein the plasma has an activity relative to the oxidizable surface;

forming an oxide film having an upper surface on the oxidizable surface;

regulating the plasma activity to limit a rate of formation of the oxide film; and

forming an oxynitride region at the upper surface of the oxide film.

68. The process of claim 67, wherein the step of forming an oxynitride region comprises subjecting the oxide film to a plasma containing a nitrogen species.

69. The process of claim 68, wherein subjecting the oxide film to a plasma containing a nitrogen species comprises subjecting the oxide film to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

70. The process of claim 67, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.

71. The process of claim 70, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.